A screenshot of a computer program

Description automatically generated

Directly implemented

Needs 2 NAND gates

Directly implemented

Needs 2 NAND gates

Needs 2 NAND gates

Needs 2 NAND gates

Needs 1 NAND gate which makes it the simplest to implement

**NAND Gate**

| **A** | **B** | **Output (A NAND B)** |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NOT Gate**

| **A** | **Output (NOT A)** |
| --- | --- |
| 0 | 1 |
| 1 | 0 |

**AND Gate**

| **A** | **B** | | **Output (A AND B)** |
| --- | --- | --- | --- |
| 0 | | 0 | 0 |
| 0 | 1 | | 0 |
| 1 | 0 | | 0 |
| 1 | 1 | | 1 |

**OR Gate**

| **A** | **B** | | **Output (A OR B)** |
| --- | --- | --- | --- |
| 0 | | 0 | 0 |
| 0 | 1 | | 1 |
| 1 | 0 | | 1 |
| 1 | 1 | | 1 |

**XOR Gate**

| **A** | **B** | **Output (A ⊕ B)** |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NOR Gate**

| **A** | **B** | **Output (A NOR B)** |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**XNOR Gate**

| **A** | **B** | **Output (A ⊙ B)** |
| --- | --- | --- |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |